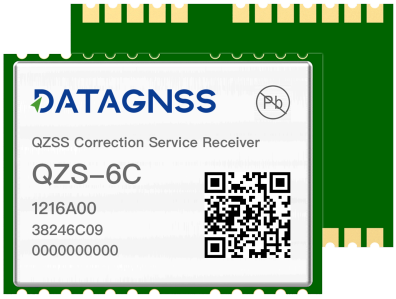
DATAGNSS

QZSS correction service receiver

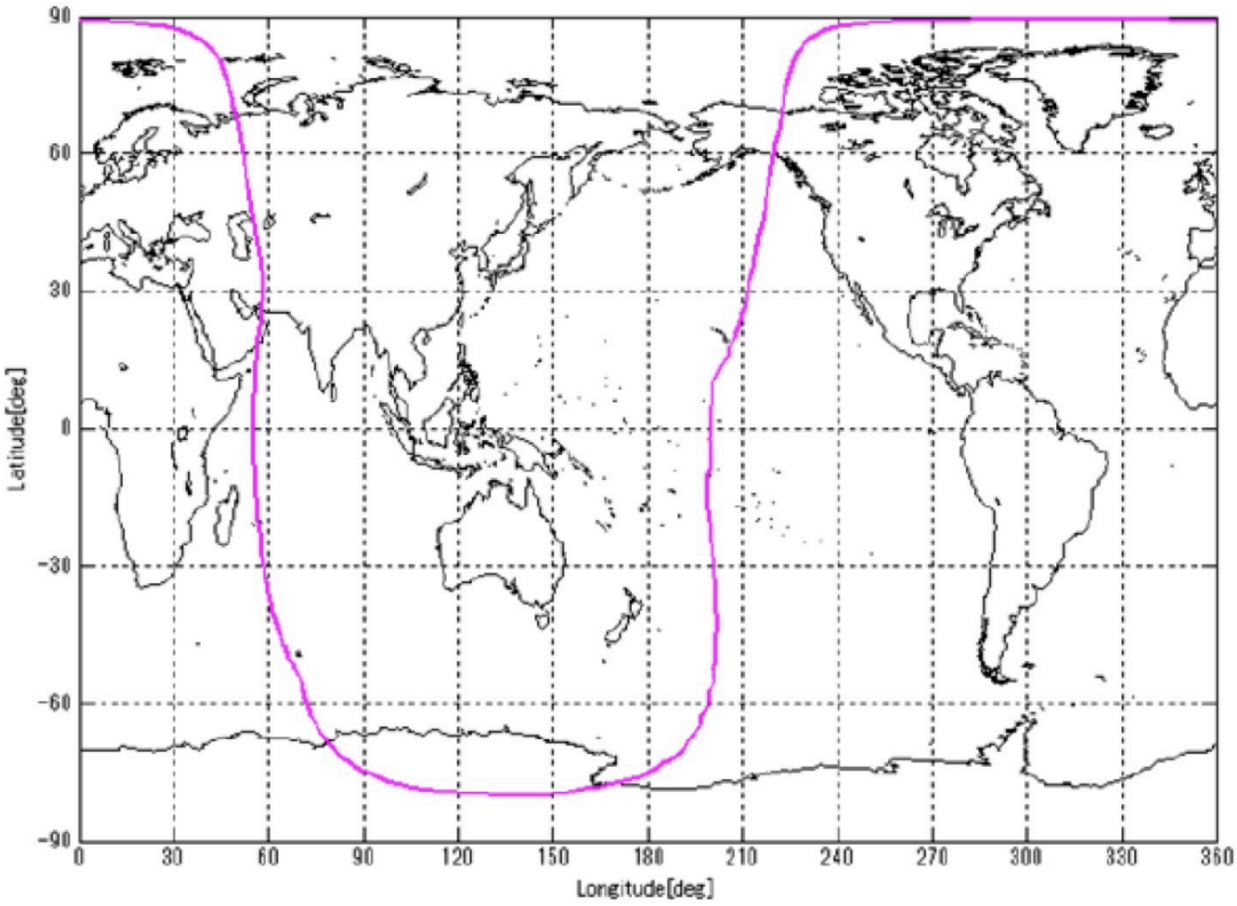
QZS-6C DATASHEET v0.9



1. SYSTEM OVERVIEW

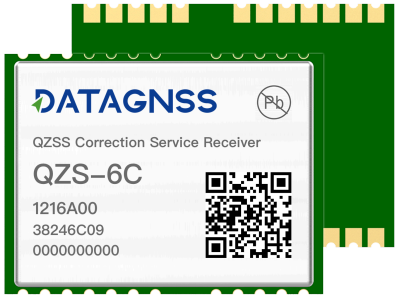
1.1 Overview

The **QZS-6C** receiver supports QZSS L6 signals, the Centimeter Level Augmentation Service (CLAS), and the experimental MADOCA service, output L6 correction service message data. The CLAS offers high-accuracy augmentation for GNSS receivers and is freely available across mainland Japan. When paired with other PPP-enabled receivers, it forms a complete, standalone high-precision system, delivering free access to high-accuracy correction services and achieving centimeter-level GNSS accuracy.



QZSS coverage area

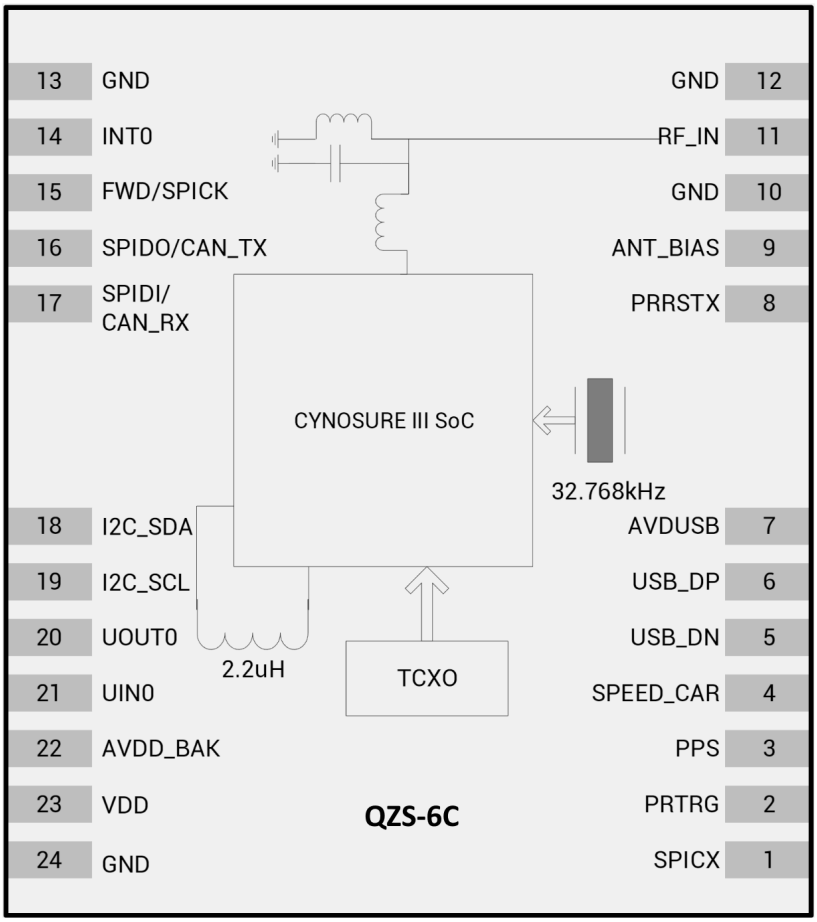
1.2 Product Photo



Order information

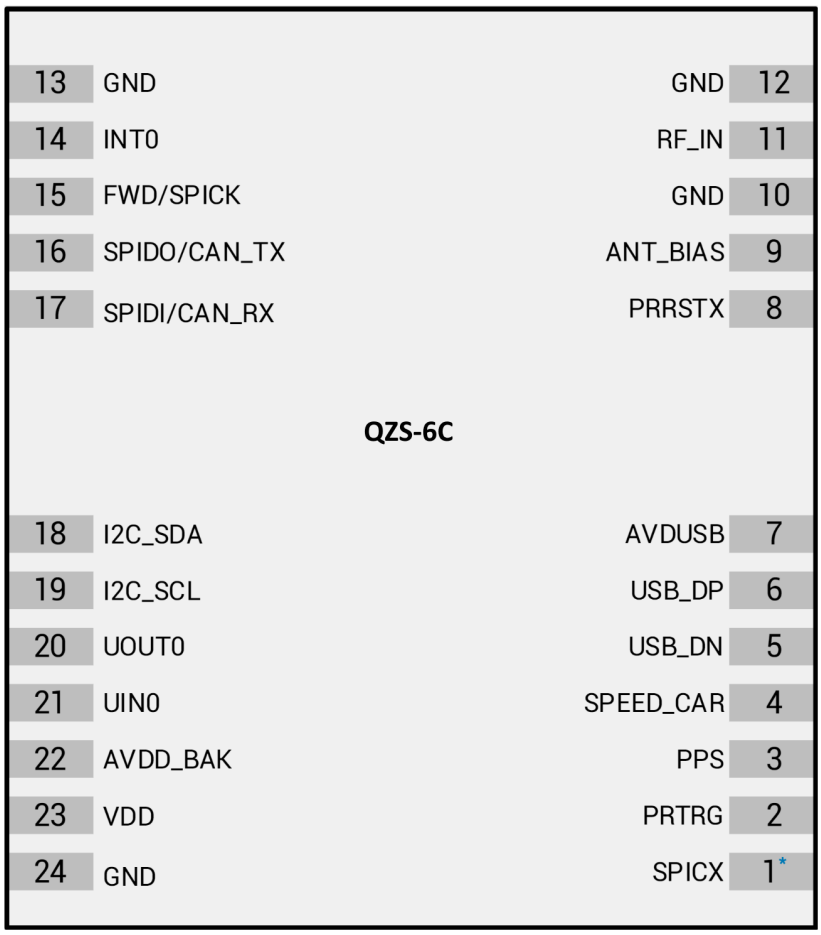
Item P/N	default configuration
QZS-6C-00	12*16mm, L1 and L6, QZSS correction service, 115200bps, default L6E firmware

1.3 Block diagram



2. PIN Definition

2.1 PINOUT



2.2 PIN description

Function	Symbol	No.	I/O	Description
Power	VDD	23	Power	Main voltage supply.
	GND	10, 12, 13, 24	VSS	Assure a good GND connection to all GND pins of the module, preferably with a large ground plane.
	AVDD_BAK	22	Power	Backup power supply voltage input.
	AVDUSB	7	Power	USB voltage supply. To use the USB interface, connect this pin to 3.0-3.6 V.
Antenna	RF_IN	11	I	Use a controlled impedance of 50Ω for the routing from RF_IN pin to the antenna or the antenna connector.
	ANT_BIAS	9	O	RF section output voltage. The ANT_BIAS pin can be used to supply powers to an external active antenna.
UART	UOUT0	20	O	UART0 serial data output.
	UIN0	21	I	UART0 serial data input.
USB[1]	USB_DN	5	I/O	USB I/O line. USB bidirectional communication pin. Leave it floating if not used.
	USB_DP	6	I/O	
SPI[1]	SPICX	1	O	SPI chip select
	FWD/SPICK	15	O	SPI clock
	SPIDO/CAN_TX	16	O	SPI data or CAN data output, leave it floating if not used.
	SPIDI/CAN_RX	17	I	SPI data or CAN data input, leave it floating if not used.
I2C[1]	I2C_SDA	18	I/O	I^2C data, leave it floating if not used.
	I2C_SCL	19	I/O	I^2C clock, leave it floating if not used.
System	PRTRG	2	I	Mode selection, or the trigger input in deep sleep mode to wake up the system
	PRRSTX	8	I	External reset, low active Connect this pin to the Host
	PPS	3	O	Time pulse output (PPS)
	SPEED_CAR[1]	4	I	Speed pulse, leave it floating if not used, default GPIO
	INT0	14	I	External interrupt, leave it floating if not used, default GPIO

3. ELECTRICAL CHARACTERISTICS

3.1 Absolute Maximum Rating

Symbol	Parameter	Min.	Max.	Unit
VDD	Power input for the main power domain	-0.5	3.63	V
AVDD_BAK	Power input for the backup power domain	-0.5	3.63	V
AVDUSB	USB supply voltage	-0.5	3.6	V
$T_{storage}$	Storage temperature	-40	85	°C
T_{solder}	Solder reflow temperature	--	260	°C

3.2 IO Characteristics

3.2.1 PRRSTX and PRTRG

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IZ}	Input leakage current	--	--	--	+/-1	uA
V_{IH}	Input high voltage	--	AVDD_BAK*0.7	--	AVDD_BAK	V
V_{IL}	Input low voltage	--	0	--	AVDD_BAK*0.3	V
C_i	Input capacitance	--	--	--	10	pF
R_{PU}	Pull-up resistance	--	18	--	84	kOhm

3.2.2 USB I/O

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IZ}	Input leakage current	--	--	--	+/-10	uA
V_{IH}	Input high voltage	--	AVDUSB*0.9	--	AVDUSB	V
V_{IL}	Input low voltage	--	0	--	AVDUSB*0.1	V
V_{OH}	Output high voltage	I_{OH} = 10 mA, AVDUSB = 3.3V	2.35	--	--	V
V_{OL}	Output low voltage	I_{OL} = 10 mA, AVDUSB = 3.3V	--	--	0.5	V
R_{PUIDEL}	Pull-up resistance, idle state	--	0.9	--	1.575	kΩ
$R_{PUACTIVE}$	Pull-up resistance, active state	--	1.425	--	3.09	kΩ

3.2.3 Others

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IZ}	Input leakage current	--	--	--	+/-1	uA
V_{IH}	Input high voltage	--	VDD*0.7	--	VDD	V
V_{IL}	Input low voltage	--	0	--	VDD*0.3	V
V_{OH}	Output high voltage	I_{OH} = 11.9 mA, VDD = 3.3V	2.64	--	--	V
V_{OL}	Output low voltage	I_{OL} = 7.9 mA, VDD = 3.3V	--	--	0.4	V
C_i	Input capacitance	--	--	--	11	pF
R_{PU}	Pull-up resistance	--	35	--	84	kOhm

3.3 DC Characteristics

3.3.1 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Power input for the main power domain	2.0	3.3	3.6	V
AVDD_BAK	Power input for the backup power domain	1.8	3.3	3.6	V
AVDUSB	USB power input	3.0	3.3	3.6	V
I_{ANT_BIAS}	ANT_BIAS output current	--	--	35	mA
V_{ANT_BIAS}	ANT_BIAS output voltage	--	VDD-0.2	--	V
ICC_{max}	Maximum operating current @ VDD	--	--	200	mA
T_{env}	Operating temperature	-40	--	85	°C

3.3.2 Power Consumption

Symbol	Parameter	Measure Pin	Typ.	Unit
I_{CCRX1}	Average tracking current (GPS/QZSS, L1 only)	VDD[1]	22	mA
I_{CCRX2}	Average tracking current (GNSS, L1+L5)	VDD[1]	34	mA
I_{CCDBM}	Standby Mode	AVDD_BAK[2]	12	uA

[1]: Condition: VDD = 3.3V @ Room Temperature; All Pins Open.
[2]: Condition: AVDD_BAK = 3.3V @ Room Temperature; All Pins Open.

4. HARDWARE DESCRIPTION

4.1 Connecting power

QZS-6C RTK receiver has two power supply pins: VDD and AVDD_BAK. The VDD pin provides the main supply voltage, and the AVDD_BAK pin provides the backup supply voltage. In order to ensure the positioning performance, please control the ripple of the module power supply. It is recommended to use the LDO with max output current above 100 mA.

If the power for VDD pin is off, the real-time clock (RTC) and battery backed RAM (BBR) are supplied through the AVDD_BAK pin. Thus, orbit information and time can be maintained and will allow a Hot or Warm start. If no backup battery is connected, the module performs a cold start at every power up if no aiding data are sent to the module.

Note: If no backup supply is available, connect the AVDD_BAK pin to VDD or leave it floating.

4.2 Power on/off Sequence

The module has two independent power domains (backup and main domain). In data backup mode, main power supply can be completely shut down for further power reduction for ultra-low power application.

To meet the requirement of controlling the power on/off sequence of the module, please connect the external reset pin (PRRSTX) to the Host.

4.2.1 Initial system power on

When both backup and main supply power on from their off state, external reset (PRRSTX) must be active and hold more than 5 ms after both backup supply and main supply reach the minimum operating voltage. Initial system power on sequence is illustrated in Figure 4.

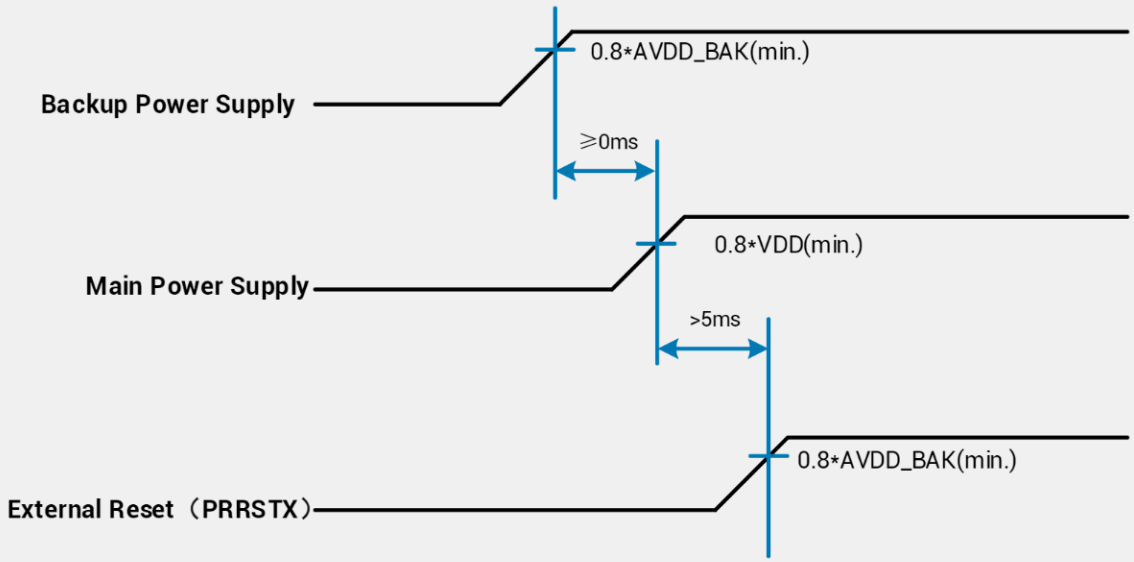
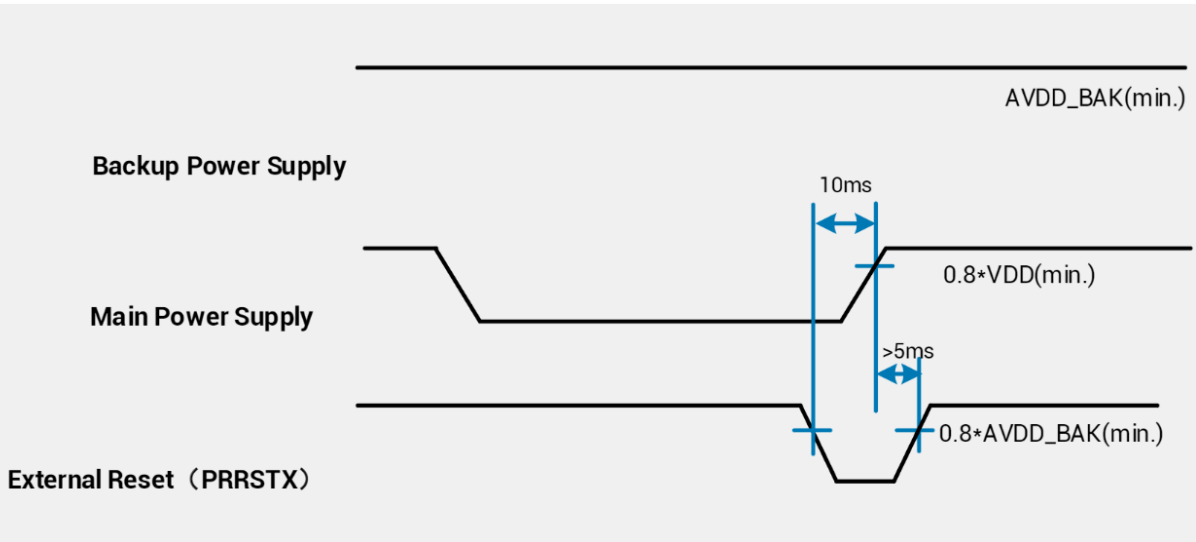


Figure 4 Initial system power on sequence

4.2.2 Main power supply off/on in application

If application intends to shut down main power supply (VDD) while keep backup power supply (AVDD_BAK) alive to save backup data, the following rules should be applied:

External reset (PRRSTX) must be active when main power supply is under power off. In this case, external reset must be hold active more than 5 ms after main power supply resumes to minimum operating voltage. Main power on sequence in application is illustrated in Figure 5.



4.3 Antenna design

There is no built-in LNA and SAW in the GNSS module. It is recommended to use an active antenna
with gain less than 50 dB and noise figure less than 1.5 dB. The module has built-in short circuit detection and open circuit detection functions, which can detect the status of normal connection, and send out antenna status prompt message in NMEA data.

- Short circuit protection
  The module includes internal short circuit antenna detection. Once an over-current is detected at the ANT_BIAS port, the module will restrict the current output automatically to protect from damage.
- Open circuit detection
  The module can detect an open circuit in the antenna. Users can judge it from antenna status messages.

Antenna status	Status output	ANT_BIAS current range
Open circuit	OPEN	0 < ANT_BIAS ≤ 1 mA
Regular circuit or open circuit	OK or OPEN	1 mA < ANT_BIAS ≤ 2 mA
Regular circuit	OK	2 mA < ANT_BIAS ≤ 40 mA
Short circuit	SHORT	ANT_BIAS > 40 mA

TIPs:

1. Pulse width of the minimum detectable overshoot current should be more than 10 uS.
2. NMEA message of antenna status output:

- OPEN: $GNTXT,01,01,01,**ANT_OPEN***40
- OK: $GNTXT,01,01,01,**ANT_OK***50
- SHORT: $GNTXT,01,01,01,**ANT_SHORT***06

4.4 Reset and mode control

The operation mode of GNSS module is controlled by PRRSTX (nRESET) and PRTRG (BOOT) pin. While the module works in normal operation, keep PRRSTX and PRTRG pins at high level. The module will enter reset state when PRRSTX being low level. Operate PRTRG and PRRSTX pins as the following instructions to enter BootROM Command Mode to update firmware.

- Keep PRTRG pin floating during system power-up or the external reset (PRRSTX from low to high), and the module will enter User Normal Mode.
- When the module powers up or PRRSTX from low to high, the module will execute an external reset. (If the power for AVDD_BAK is always on, the external reset will not affect the ephemeris data in the backup domain)
- Drive PRTRG pin to low or connect PRTRG to GND directly (not by pull-down resistance) during system power-up or the external reset (PRRSTX from low to high), and the system enters BootROM Command Mode at PRTRG pin being released from low to floating state, and ready for firmware upgrading command.
- When connecting PRRSTX and PRTRG to any host IO, DO NOT use the pull-up or pull-down resistance

5. DEFAULT MESSAGE

5.1 Default configuration

UART OUTPUT	115200 baud, 8 data bits, no parity bit, 1 stop bit Configured to transmit both NMEA and L6 Raw data
UART INPUT	115200 baud, 8 data bits, no parity bit, 1 stop bit, autobauding disabled Automatically accepts the following protocols without need of explicit configuration: Binary sentence, NMEA, RTCM.
Timepulse	1 PPS, synchronized at rising edge, pulse length 100 ms

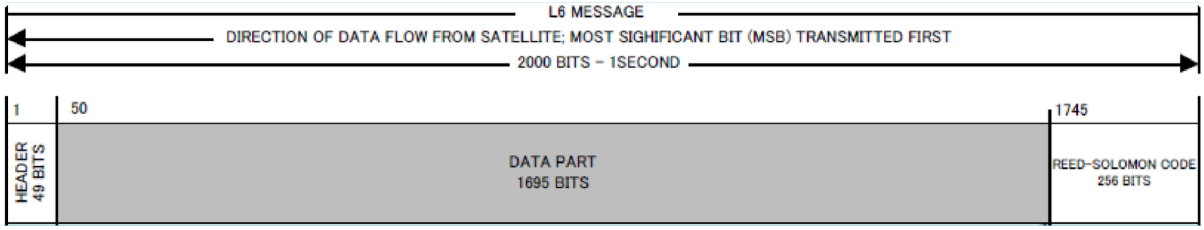
When the module is applied to the specific application where the main supply needs to be cut, in this case, it is recommended to cut the serial interface connection at the same time or set the serial port to input mode or high impedance state

5.2 L6 Message data

The L6 data is transmitted from the satellites in 250-symbol subframes with duration of 1000 ms. Each subframe starts with a fixed 4-symbol preamble (0x1A, 0xCF, 0xFC, 0x1D), followed by 214 data symbols and 32 Reed-Solomon parity symbols. This message structure applies to both L6D and L6E signals.

The detailed explanation of the L6 message is in this document: IS-QZSS-L6-001 specification for the QZSS L6D/E service.

The **QZS-6C** receiver only receives and forwards L6 data without parsing, processing, or other actions. To achieve subsequent PPP data processing, other models of products are required. For details, please refer to other products at www.datagnss.com.



Message	RAWX-QZSSL6					
Description	QZSS L6 correction data					
Message structure	Header	Group	ID	Length(Bytes)	Payloads	Checksum
	0xF1D9	**0x02**	**0x10**	2	**see below**	**CK_1 CK_2**

Payload contents				
Byte offset	Type		Unit	Description
0	U2	SVN	-	QZSS L6 SVN, 700+prn.
2	U1	Freq ID	-	0.
3	U1	Data length	-	word size, value=N+2
4	U2	GNSS Week Number	-	Number of GNSS week
6	U4	TOW	ms	-
10	U1	SNR	-	Message version, 0x03
11	U1	Flag	-	QZSL6_ALL_GOOD: 0x00 QZSL6_RS_FAILED: 0x01 QZSL6_WEEK_NOT_CONFIRM: 0x02 QZSL6_TOW_NOT_CONFIRM: 0x04
12	U1[N*4]	msgByts	-	L6 message data, N=63

[1] IS-QZSS-L6-001: https://qzss.go.jp/en/technical/download/pdf/ps-is-qzss/is-qzss-l6-001.pdf
[2] MALIB PPP support QZS-6C receiver, https://github.com/JAXA-SNU/MALIB

6. MECHANICAL SPECIFICATION

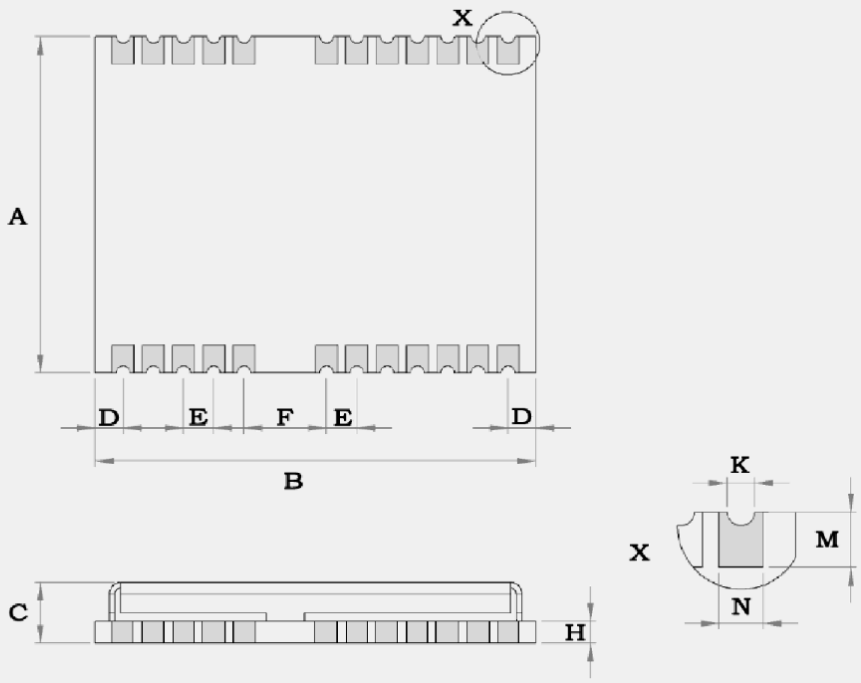


Figure 6 Dimensions

Table 13 Dimensions

Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	12.0	12.2	12.4
B	15.8	16.0	16.2
C	2.2	2.4	2.6
D	0.9	1.0	1.3
E	1.0	1.1	1.2
F	2.9	3.0	3.1
H	--	0.8	--
K	0.4	0.5	0.6
M	0.8	0.9	1.0
N	0.7	0.8	0.9

7. REFERENCE DESIGN

7.1 Minimal design

This is a minimal design for the QZS-6C GNSS module. The 82 nH inductor is used only when an active antenna is connected, and no need with a passive antenna. The characteristic impedance from RF_IN pin to the antenna connector should be 50Ω.